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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER

PATHAK, SUDHANSHU C

ART UNIT PAPER NUMBER

2634

DATE MAILED: 05/19/2004

8

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/982,267

Applicant(s)

GAY-BELLILE ET AL.

Examiner

Sudhanshu C. Pathak

Art Unit

2634

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on March 23rd, 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-15 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-15 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on March 23rd, 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- ☐ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- ☐ Notice of Informal Patent Application (PTO-152)
- ☐ Other: _____

DETAILED ACTION

1. Claims 1-to-15 are pending in the application.

Claim Objections

2. The numbering of claims is not in accordance with 37 CFR 1.126 which requires the original numbering of the claims to be preserved throughout the prosecution. When claims are canceled, the remaining claims must not be renumbered. When new claims are presented, they must be numbered consecutively beginning with the number next following the highest numbered claims previously presented (whether entered or not). Misnumbered claim 13 has been renumbered 12 and the claims following the misnumbered claim have also been re-numbered.

Claim Rejections - 35 USC § 101

3. 35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

4. Claims 6 & 10 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The subject matter claimed is "a signal for carrying a computer program", a signal in itself is unpatentable, but a method and an apparatus to generate the desired signal are patentable.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 5 & 9 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 5 & 9 are hybrid claims. The claims should either describe an apparatus for a particular function or a method for carrying out a process. Both method and an apparatus cannot be specified in the same claim. Both claims 5 & 9 describe a "computer program product", however both the claims are dependent on claim, which describes "a method of channel decoding". Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claims 1, 3, 4, 7-8, 10-13 & 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Uchida (EP-0966157 A1) in view of Stott et al. (6,240,146) in further view of Garde et al. (5,685,005).

Regarding to Claims 1, 3, 4, 7-8, 10-13 & 15, Uchida discloses a receiver and a receiving method configured to receive signals of a plurality kinds of communications media (Column 1, lines 1-4). The receiver described in Uchida is used for enabling a television receiver to cope with multiple communication signals (Column 1, lines

12-58 & Figure 6A & B). The communications signals can be transmitted by conventional broadcastings, satellite broadcastings, digital CATV, and through the internet (Column 1, lines 23-42). The basic structure of the receiver consists of a front-end processing and back-end (common) processing (Figure 1). Uchida describes front-end processing to include demodulation, forward error correction (FEC), or processing specific to the type of communication signal received (Figure 1 & Column 3, lines 31-45 & Column 7, lines 23-57 & Figure 7). Uchida also discloses completing the front-end processing before sending data to the common processor (Column 4, lines 9-10). Uchida discloses a common processor for performing processing common to all the different kinds of communications media (Column 2, lines 33-37 & Figure 7). Uchida further discloses implementing multiple front end processing units for processing various different signals and communicating the output with the common processor (Figure 6A & B). Uchida further discloses the common processor to include a central processor for managing control and configuration (Column 8, lines 45-55 & Figure 7). However, Uchida does not specify the front-end processing to include channel correction and further does not disclose a memory shared between the front-end processes and the common processor.

Stott discloses an apparatus for demodulating digital video broadcast signals (Column 1, lines 6-26). Stott further discloses the demodulating apparatus to include a channel correction block (Figure 2, element 32 & Figure 4, element 32). Stott further discloses implementing the processing functions in hardware and software (Column 4, lines 10-25 & Column 10, lines 37-46). Therefore, it would

have been obvious to one of ordinary skill in the art at the time of the invention that implementing the channel correction block as described in the receiver in Stott to the front-end of the receiver as described in Uchida would improve the accuracy of the data and increase the data rate in various different channel environments, by compensating for the communication channel impairments. However, Uchida in view of Stott does not disclose implementing a shared memory scheme between the front-end processors and the common processor.

Garde discloses a digital signal processor (DSP) architecture to optimize performance for applications such as fast Fourier transforms (FFT), digital filters, image and speech processing (Column 1, lines 10-22). Garde discloses a signal processing system comprising a first DSP and a second DSP interconnected to the first DSP by an external bus (Column 1, lines 39-43). Garde also discloses implementing a shared memory scheme between the first and second DSP and further assigning memory depending on the processor ID (Column 1, lines 39-67 & Column 2, lines 1-35). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention that implementing the multiple signal processors as described in Garde in the receiver as described in Uchida in view of Stott would enhance the performance of the receiver by increasing the computation rate of the processors and thus increase the data rate of the receiver and further would provide increased integration of the periphery circuitry, reduce the overall cost and complexity of the receiver. Furthermore, breaking the processing tasks between

the processors depending on the functionality or data formats is a matter of design choice and there is no criticality in the breakdown of the processing functions.

9. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Uchida (EP-0966157 A1) in view of Stott et al. (6,240,146) in further view of Garde et al. (5,685,005) in further view of Nicolas et al. (5,453,797).

Regarding to Claim 2, Uchida in view of Stott in further view of Garde discloses a receiver and a receiving method configured to receive signals of a plurality kinds of communications media as described above. Uchida describes front-end processing to include demodulation, forward error correction, or processing specific to the type of communication signal received (Figure 1 & Column 3, lines 31-45 & Column 7, lines 45-57 & Figure 7). Uchida further discloses base-band demodulation of the received signal (Figure 7, elements 100 & 101 & Column 7, lines 30-33). Stott describes a receiver receiving and demodulating a digital video broadcast signal-comprising data modulated on a multiplicity of a spaced carrier frequencies (Column 1, lines 60-67) including coded orthogonal frequency division multiplexing (COFDM) (Column 1, lines 8-26). Stott further discloses implementing a FFT for performing demodulation in case of multi-carrier systems (Column 1, lines 27-29 & Figure 2, element 24). Stott also discloses loops for time and carrier recovery (Figure 1, element 9 & Figure 2, elements 38, 40, 9 & Figure 2, elements 26, 28, 8). Stott also discloses a FEC decoder for decoding convolutionally coded data (Column 1, lines 18-23 & Figure 1, element 10). Stott further discloses an adaptive filter array for time domain equalization (Figure 2, elements 30 & Column 5, lines 9-14). Stott

further discloses gain control loop to preserve the linearity so as not to create intermodulation products between the carriers (Column 6, lines 3-12). Stott also discloses interference rejection and frequency interpolation (Figure 5, element 38 & Column 7, lines 31-38). However, Uchida in view of Stott in further view of Garde does not specify a programmable nyquist filter, a Reed-Solomon decoder and frequency domain equalization.

Nicolas discloses a receiver used in high definition television (HDTV) systems (Column 1, lines 9-12) comprising a programmable nyquist filter for demodulating the received signal (Figure 2, element 206 & Column 3, lines 14-25 & Column 4, lines 62-67), a slicer for decoding a Reed-Solomon code (Figure 2, element 214 & 28-33) and a frequency domain equalizer (Figure 2, element 210 & Figure 12).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention that by implementing the nyquist filter, equalizer and the reed-solomon decoder as described in Nicolas into the receiver as described in Uchida in view of Stott in further view of Garde would enhance the quality of the data received by the receiver and furthermore would allow the receiver to receive both single carrier and multi-carrier modulated data.

10. Claims 5, 9 & 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Uchida (EP-0966157 A1) in view of Stott et al. (6,240,146) in further view of Garde et al. (5,685,005) in further view of Sarfati (6,478,222).

Regarding to Claims 5, 9 & 14, Uchida in view of Stott in further view of Garde discloses a receiver and a receiving method configured to receive signals of a

plurality kinds of communications media as described above. However, Uchida in view of Stott in further view of Garde does not disclose a computer program product which when downloaded into the receiver causes the receiver to carry out the instructions.

Sarfati discloses a method for downloading an executable application into a decoder for a digital broadcast receiver to permit the processing of the received data (Abstract, lines 1-11). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention that by implementing the method of downloading a set of instructions into the receiver to carry out the method as described in Uchida in view of Stott in further view of Garde provides the data to be received and automatically decoded depending on the transmitted signal. Furthermore, breaking the processing tasks between the processors depending on the functionality or data formats is a matter of design choice and there is no criticality in the breakdown of the processing functions.

Response to Arguments

11. Applicant's arguments filed on March 23rd, 2004 have been fully considered but they are not persuasive.

In regards to arguments regarding the Claims, Uchida discloses a receiver structure comprising multiple front-end processing units and a common processing unit (Fig. 1 & Abstract, lines 1-14). Uchida also discloses that each front end to comprise processor(s) for processing functions specific to the communications signals received such as television receiver sets, satellite

broadcasting, cable television, internet etc. (Fig. 1, Column 1, lines 10-46 & Column 3, lines 20-58 & Column 4, lines 1-6). Uchida also discloses that the front end processing unit receives the RF (analog) signal and provides a data stream such as MPEG-2 transport stream to the common processor (Fig. 7, element 3 & Column 3, lines 48-51). Uchida further discloses the front end processing to include analog processing, digital demodulation, forward error correction (FEC), and decoding (Column 7, lines 23-58 & Fig. 7). Uchida also discloses that the data provided to the common processor unit is in packet form for further processing (Column 8, lines 8-44 & Fig. 7, element 5). Uchida further discloses the common processor for controlling and processing of the received data so as to display the data in an appropriate format (Column 8, lines 8-58). Therefore, the front-end processing units as described in Uchida are analogous to the cluster of coprocessors for executing the function of error correction, digital front end processing or any function specific to the incoming signal standard and the common processing unit is analogous to the general purpose processor of the claims. Furthermore, it would have been obvious to one of ordinary skill in the art at the time of the invention that the front-end processing as disclosed in Uchida is analogous to layer-1 and layer-2 processing of a signal processing implementation. Furthermore, it is also obvious that these functions are implemented in a DSP which is programmable and code has to be stored to process the digital data with error correction, digital demodulation, decoder, channel estimation etc. The coprocessors and general-purpose processor as

described in claims perform the same functions performed in the front-end units and the common processing unit as described in Uchida, and therefore, they are analogous.

The Stott reference discloses channel estimation and correction as one of the functions, which are not explicitly specified in the Uchida reference, in the receiving and processing chain of broadcast signals (Column 9, lines 63-67 & Column 10, lines 1-38 & Fig. 2, element 32 & Fig. 4, element 32). Furthermore, Stott also refers to the functions performed (processing) as DSP operations (Column 4, lines 10-25) therefore; they can be implemented in a digital signal processor, which is programmable. Therefore, Uchida in view of Stott discloses all the processing functions described in the claims to be performed on the received signals.

The Garde reference discloses a DSP architecture comprising a shared memory scheme between the first and second DSP and further assigning memory to respective processors depending on the processor ID (Column 1, lines 39-67 & Column 2, lines 1-35), which is not explicitly specified in the Uchida in view of Stott references. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention that this architecture can be implemented between the processors as disclosed in the Uchida references. Thus, Uchida in view of Stott in further view of Garde satisfies all the recited limitations of the claims. Uchida in view of Stott discloses a set of processors for performing the functions of the claim and Uchida further discloses a general-purpose processor

for managing control and configuration and Garde discloses the shared memory architecture so as to implement the processing.

The Sarfati reference discloses a method for downloading an executable application into a decoder for digital broadcast receiver to permit the processing of the received data (Abstract, lines 1-11), and these downloaded instructions can be programming the decoding functions into the processors as recited in the claims.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sudhanshu C. Pathak whose telephone number is (703) 305-0341. The examiner can normally be reached (Monday-Friday from 8:30 AM to 5:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin, can be reached at (703) 305-4714.

Any response to this action should be mailed to:

- Commissioner of Patents and Trademarks Washington, D.C. 20231

Or faxed to:

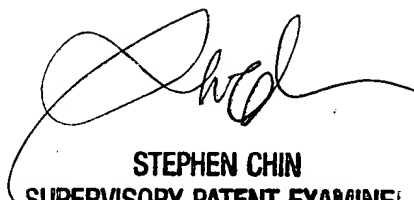
- (703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to:

- Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor
(Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to:

- Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.



STEPHEN CHIN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600